High Aspect Ratio Single Crystalline Silicon Microstructures Fabricated With Multi Layer Substrates

C. Gui, H. Jansen, M. de Boer, J. W. Berenschot, J. G. E. Gardeniers and M. Elwenspoek
MESA Research Institute, University of Twente
P. O. Box 217, 7500 AE Enschede, The Netherlands, Email: c.gui@el.utwente.nl

SUMMARY

This paper reports a new method for making high aspect ratio Single Crystalline Silicon (SCS) microstructures on multi layer substrates using Chemical Mechanical Polishing (CMP), Silicon Fusion Bonding (SFB) and Reactive Ion Etching (RIE) techniques. First Si-SiO_2-PolySi-SiO_2-Si sandwich wafers were fabricated using CMP and SFB. Then microstructures were fabricated on these sandwich wafers using an one run self-aligned RIE process, where polysilicon was used as the sacrificial layer. Polishing and bonding of Low Pressure Chemical Vapour Deposition (LPCVD) polysilicon were studied. A LPCVD $Si_{3+x}N_4$ polishing stop layer technique was developed to accurately control the final thickness of the device layer. The uniformity of the device layer was improved as well.

Keywords: Silicon Fusion Bonding, Chemical Mechanical Polishing, Reactive Ion Etching

INTRODUCTION

Up to date, the process incorporating SFB in making free-standing microstructures can be distinguished in two technique routes: 1) "cavity" etching before bonding [e.g. 1-5], and 2) sacrificial layer etching after fusion [e.g. 6-8]. The convenience of etching a cavity before bonding is that the gap defined by the depth of the cavity could be as large as necessary without the constraint of the thickness of the sacrificial layer. The drawback is, however, that at least two masks are necessary to make a micro mechanical structure. On the other hand, fabricating micro structures from sandwich wafers (e.g. Silicon-On-Insulator (SOI) wafers) using the sacrificial layer etching technique enables self-alignment fabrication. In this technique, the structures are patterned and etched by RIE on the top silicon layer of the SOI wafer. Then the structures are released by wet or dry isotropic etching.

When using the combination of SFB and RIE technologies in fabricating SCS structures with high aspect ratio, RIE lag was found to be a problem [5]. Furthermore, the thickness and the uniformity of the top silicon layer having a thickness of several tens of micrometers were not controllable due to the lack of a stop layer, which will cause problems during releasing the microstructures.

Here we propose a different technique. SCS microstructures were made from Si-SiO_2-PolySi-SiO_2-Si sandwich wafers. LPCVD polysilicon was used as the sacrificial layer which enables the one run self-aligned process. A thin oxide layer was introduced between the device layer and the sacrificial layer as a etch stop layer, due to the high etch selectivity of silicon to silicon dioxide (200:1). An LPCVD $Si_{3+x}N_4$ CMP stop layer technique was introduced to control the final thickness as well as to eliminate the nonuniformity of the device layer across the whole wafer.

THE MULTI LAYER SUBSTRATES

Previously, we have demonstrated the multi step one run self-aligned RIE process on commercial BESOI wafers [8]. The commercial BESOI wafers which were optimised for IC's were found not always suitable for fabricating microstructures. Also polysilicon structures with limited aspect ratio were realised on wafers having PolySi-SiO_2-PolySi-SiO_2-Si sandwich layers. In order to make SCS microstructures, Si-SiO_2-PolySi-SiO_2-Si sandwich wafers have to be fabricated in the first hand.

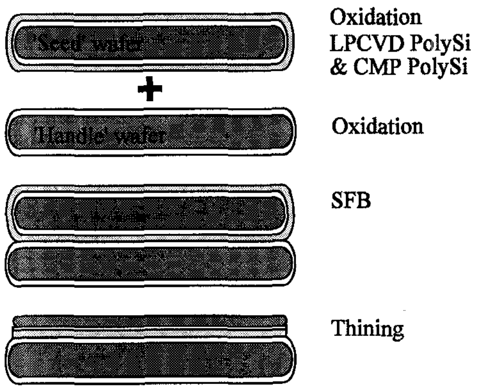

Fig. 1, Process sequence of the Si-SiO_2-PolySi-SiO_2-Si sandwich wafers

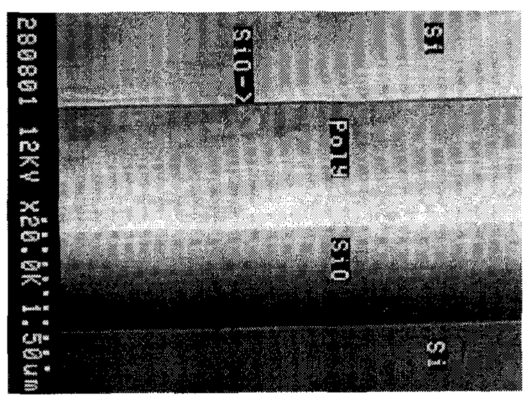

Fig. 2, SEM image showing the cross section of an Si-SiO_2-PolySi-SiO_2-Si sandwich wafer

The process of fabricating the Si-SiO_2-PolySi-SiO_2-Si sandwich wafers started with growing a thin (50 to 200 nm thick) thermal oxide layer on top of a 3 inch, double side polished, (100) oriented silicon wafer, or 'seed' wafer. Then a several micrometers thick LPCVD polysilicon layer was deposited on top of the oxidized wafer. A 1 hour anneal at 1100 °C in N_2 was conducted to release the stress inside the polysilicon layer. After CMP of the LPCVD polysilicon, the 'seed' wafer was cleaned and fusion bonded to a 'handle' silicon wafer that was covered with a 1 μm thick thermal oxide layer. The bonded wafer pair was annealed for 2 hours at 1150 °C. The 'seed' wafer was thinned to the desired thickness by means of KOH etching followed by a brief CMP step. The fabrication process of the multi layer wafers is graphically shown in Fig. 1. An SEM photo showing the cross section of a sandwich wafer is presented in Fig. 2.

POLISHING AND BONDING OF LPCVD POLYSILICON

Polishing and bonding LPCVD polysilicon has been reported before, e.g. for micro accelerometers [9] and dielectric isolation applications [10, 11]. However there was no detailed descriptions on the LPCVD polysilicon polishing and bonding process.

An CMP step is a must before the LPCVD polysilicon layer can be successfully bonded to a silicon wafer or an oxidised silicon wafer. The Root Mean Square (RMS) roughness of the LPCVD polysilicon layer before CMP was measured to be between 5 to 15 nm, which is much higher than the 0.5 nm that is widely believed to be the critical RMS roughness of a bondable surface. Further more, the polysilicon layer was covered with many protruding particles of several tens to 100 nm high (see Fig. 3).

The CMP process was optimised for LPCVD polysilicon polishing with respect to the pads, the slurries and the process parameters such as the work pressure, pad temperature, the rotating speed, etc. The slurries and pads for final polishing of SCS wafers can be used to polish LPCVD polysilicon. However the removal rate of LPCVD polysilicon was found to be more than 5 times higher than that of SCS (100), if the same process procedure is applied. We also found that the removed amount of LPCVD polysilicon does not have to be large. As soon as the protruding particles on the LPCVD polysilicon surface are removed, the CMP process should be stopped. Longer polishing will lead to the formation of pits on the polished LPCVD polysilicon surface. LPCVD polysilicon grain boundaries are believed to be removed faster than the silicon crystals themselves. Also polysilicon grains of different orientation are removed at different rates [12]. When final polishing slurry LS 10 and final polishing pad UR 100 were used, mirror-like polysilicon surfaces were achieved within 3 minutes CMP at a reasonable removal rate of about 30 nm/min. The surface topographies of the LPCVD polysilicon before and after CMP are shown in Fig. 3. The resulting RMS roughness of the polysilicon surface measured by Atomic Force Microscopy (AFM) was typically 0.3 to 0. 4 nm.

The room temperature bonding process was monitored with an infrared camera. After the first contact, an immediate bonding between the polished polysilicon layer and the oxidized wafer was observed. The propagating speed of the bond wave over the whole wafer was measured to be about 3 cm/min. Transmission Electron Microscopy (TEM) shows a well bonded interface between polysilicon and silicon dioxide (Fig. 4).

The resulting room temperature bond strength between polysilicon to silicon dioxide varied from 0.04 to 0.1 J/m^2, which is in the same range as that of silicon hydrophilic bonding. There is always a thin native silicon oxide layer covered on top of the polysilicon layer, just like that on SCS surface. So, we believe that the bonding mechanism between the polysilicon layer to the silicon dioxide layer is the same as that between SCS to silicon dioxide.

FABRICATION OF THE MICRO STRUCTURES

After fabricating the multi layer substrate, a high density RIE process [13] was used in etching and defining the structures. Then, several releasing process are possible in freeing the microstructures.

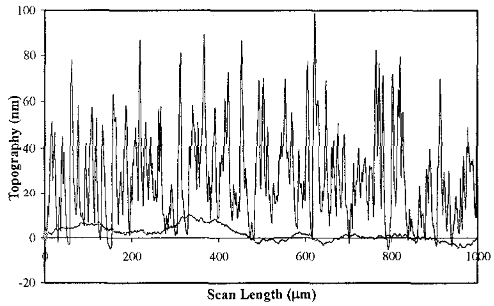

Fig. 3, Surface topographies of the LPCVD polysilicon before (rough line) and after (smooth line) CMP

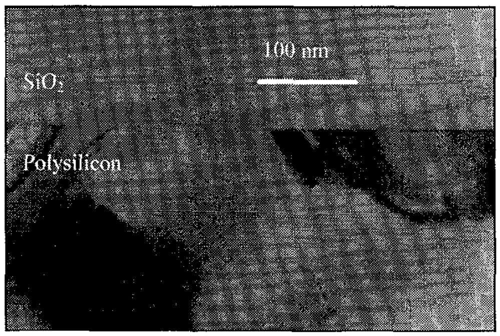

Fig. 4, TEM image showing the bonding interface between LPCVD polysilicon and SiO_2

Here the movable structures were fabricated in only one RIE run with four individual steps, see [8]. The fabrication sequence is shown in Fig. 5. Free-standing cantilever beams, clamped-clamped beams and circular rings were made (Fig. 6, 7). The demonstrated structures were 25 μm high. The gap size was 1.6 μm. However, the thickness combinations of the top device layer and the sacrificial layer are freely selectable. High aspect ratio SCS structures are only constrained by the RIE process where etching of hundreds micrometers deep structures are possible today [14].

No stiction was observed in these structures. This is one of the advantages of the dry releasing technique. No stress caused by the bonding interface was found. The bonding interface was not preferentially etched during RIE process. In fact, it has the same behaviour as the deposition interface during etching.

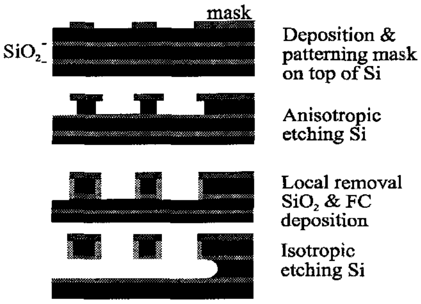

Fig. 5, Processes of fabricating microstructures on the multi layer substrate using the one run RIE technique

CMP STOPPER TECHNIQUES

During etching back of the bonded multi layer substrates, one can not achieve a precise required thickness of the top device layer with only a time stop during KOH etching. The resulting Total Thickness Variations (TTV) of the device layer after KOH etching without a stop layer are normally several micrometers, sometimes even larger than 10 micrometers, depending on the TTV of the seed wafer and the performance of the KOH etching process.

The CMP removal rate of LPCVD $Si_{3+x}N_4$ layer is 10 to 30 times lower than that of a SCS (100) wafer. Therefore LPCVD $Si_{3+x}N_4$ layer has been frequently used as a polishing stopper in making SOI wafers having a top device layer of hundreds of nanometers to several micrometers thick [15]. We propose to use LPCVD $Si_{3+x}N_4$ structures incorporated in the device wafer as an CMP stopper to accurately control the thickness and uniformity of the top device layer of several tens of micrometers thick.

The fabricating sequence for making the multi layer wafers with an LPCVD $Si_{3+x}N_4$ polishing stop layer is shown in Fig. 8. First, narrow and deep trenches were etched using RIE and filled with LPCVD $Si_{3+x}N_4$ layer in the "seed" silicon wafer. The depth of these trenches defines the thickness of the device layer. $Si_{3+x}N_4$ layer on top of the silicon wafer was removed using RIE. Then a thin thermal oxide layer and an LPCVD polysilicon layer were deposited. After a brief CMP of the polysilicon, the 'seed' wafer was fusion bonded to a 'handle' silicon wafer that covered with a thermal oxide layer. The 'seed' wafer was thinned till the stop layer by wet etching and CMP. To date, we are able to achieve a less than 1 μm TTV of the top Si layer. A cross section of the trench filled with $Si_{3+x}N_4$ CMP stop layer is shown in Fig. 9.

CONCLUSION

We have developed a new technique of making Si-SiO_2-PolySi-SiO_2-Si sandwich wafers using CMP and SFB. Direct bonding between LPCVD polysilicon and silicon dioxide with good quality has been obtained after a brief polishing the polysilicon surface using the optimised CMP process. An LPCVD $Si_{3+x}N_4$ polishing stop layer technique has been developed to control the thickness and improve the uniformity of the top device layer. High aspect ratio SCS microstructures have been fabricated from the multi layer substrates using the one run RIE process. This technology offers following advantages: 1) SCS microstructures made from the sandwich wafers offer

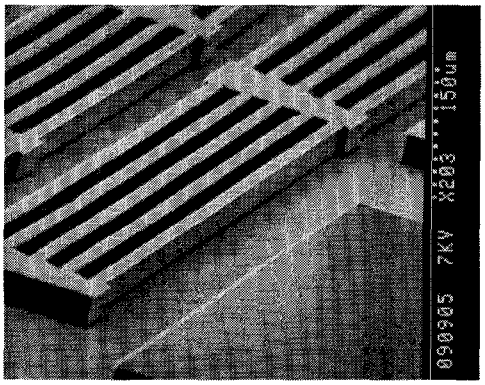

Fig. 6, SEM photo showing free-standing clamped-clamped beams made from the multi layer substrate

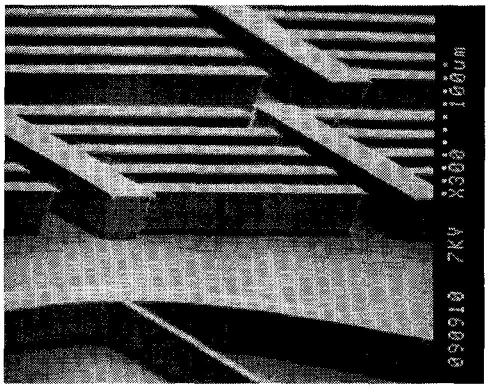

Fig. 7, SEM photo showing free-standing cantilever beams and part of the rings made from the multi layer substrate

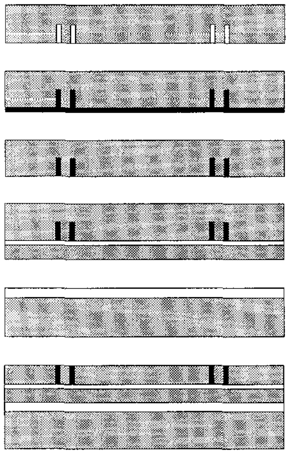

Fig. 8, Process sequence of fabricating multi layer substrate with CMP stop layer

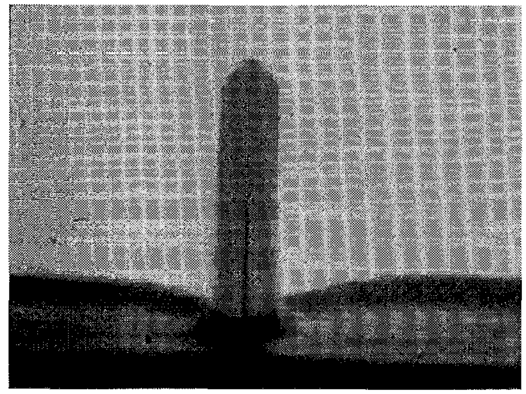

Fig. 9, LPCVD $Si_{3+x}N_4$ embedded in silicon wafer as CMP stop layer

good mechanical properties; 2) The thickness combinations of the top device layer and the sacrificial layer are freely selectable and high aspect ratio SCS microstructures are only constrained by the RIE process where etching of hundreds μm deep structures are possible today; 3) No stiction was observed in the microstructures released on the sandwich wafers using the one run self-alignment process; 4) The top thinner oxide layer, used as a stop layer, facilitates the anisotropic RIE lag problem; while the bottom thicker oxide layer provides sufficient electrical isolation together with a smooth bottom; And 5) this technique is IC process compatible.

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